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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/688,933 | 10/17/2000 | Koichi Takiguchi | 32307-167197 | 2516 |

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VENABLE, BAETJER, HOWARD AND CIVILETTI, LLP
P.O. BOX 34385
WASHINGTON, DC 20043-9998

| EXAMINER | |
|---|---|
| PHAN, HANH | |
| **ART UNIT** | **PAPER NUMBER** |
| 2633 | 10 |

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/688,933 | TAKIGUCHI ET AL. | |
| | Examiner | Art Unit | |
| | Hanh Phan | 2633 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 October 2000*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6 and 15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7 & 8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 03/05/2004.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taga et al (US Patent No. 6,181,449) in view of Jinguji et al (US Patent No. 5,572,611).

Regarding claims 1 and 15, referring to figure 1, Taga discloses a dispersion slope equalizer (i.e., dispersion equalizer elements 5, Fig. 1) for compensating signal distortion caused by dispersion slope of a transmission line when transmitting lightwaves with plural wavelength signals in the transmission line characterized by comprising:

N waveguides, N output wavelength demultiplexer and/or N input wavelength multiplexer (Fig. 1), and the N waveguides being connected to outputs of the wavelength demultiplexer (i.e., arrayed optical waveguide wavelength demultiplexing circuit 3, Fig. 1) and/or inputs of the wavelength multiplexer (i.e., arrayed optical waveguide wavelength multiplexing circuit 4, Fig. 1)(from col. 3, line 45 to col. 5, line 9).

Taga differs from claims 1 and 15 in that he fails to teach K (K<N) group delay controllers and in the group delay controllers, one or both of input/output parts of lattice-form optical circuits being set on the N waveguides wherein the lattice-form optical circuits are composed of two waveguides interleaved with at least two directional couplers, and the two waveguides are designed so that optical path lengths between the directional couplers are different. However, Jinguji in US Patent No. 5,572,611 teaches a dispersion slope equalizer comprising group delay controllers and in the group delay controllers, one or both of input/output parts of lattice-form optical circuits being set on the N waveguides wherein the lattice-form optical circuits are composed of two waveguides interleaved with at least two directional couplers, and the two waveguides are designed so that optical path lengths between the directional couplers are different (Fig. 3, col. 53, lines 44-60 and see abstract section). Although Jinguji does not specifically teach K group delay controllers comprising lattice-form optical circuits connected to N waveguides (K: natural number, K<N). However, Jinguji teaches a lattice-form variable group delay dispersion equalizer has two inputs (5,6) and two outputs (7,8) (as indicated in Fig. 3, column 3, lines 50-67 and col. 4, lines 1-14). Whether to use one input and one output of a lattice-form variable group delay dispersion equalizer connect to one waveguide ( where K lattice-form variable group delay dispersion equalizers = N waveguides with K=N) or to use two inputs and two outputs of a lattice-form variable group delay dispersion equalizer connect to two waveguides (where K lattice-form variable group delay dispersion equalizers = N/2 waveguides with K<N) would have been within the knowledge of a person having

ordinary skill in the art and would have been an obvious engineering design choice. Therefore, it would have been obvious to obtain K group delay controllers comprising lattice-form optical circuits connected to N waveguides (K: natural number, K<N) in order to allow the amount of dispersion equalizers used can be cut down, reducing the size, weight and cost of the system. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to incorporate the variable group delay dispersion equalizer using lattice form as taught by Jinguji in the system of Taga. One of ordinary skill in the art would have been motivated to do this since Jinguji suggests in column 3, lines 50-67 and col. 4, lines 1-14 that using such a variable group delay dispersion equalizer using lattice form has advantage of allowing compensating the dispersion of the signal and to be able to reduce the amount of dispersion equalizers used, reducing the size, weight and cost of the system.

Regarding claims 2 and 16, Taga further teaches the wavelength demultiplexer (3) and wavelength multiplexer (4)(Fig. 1) are arrayed-waveguide gratings.

Regarding claims 3 and 17, the combination of Taga and Jinguji teaches the group delay controllers are connected to N input wavelength multiplexer and the N waveguides are connected to only inputs of the wavelength multiplexer (Fig. 1 of Taga and Fig. 3 of Jinguji).

Regarding claims 4 and 18, Taga further teaches the wavelength multiplexer (4)(Fig. 1) is an arrayed-waveguide grating.

Regarding claims 5 and 19, the combination of Taga and Jinguji teaches the group delay controllers are connected to N output wavelength demultiplexer and the N

waveguides are connected to outputs of the wavelength demultiplexer (Fig. 1 of Taga and Fig. 3 of Jinguji).

Regarding claims 6 and 20, Taga further teaches the wavelength demultiplexer (3)(Fig. 1) is an arrayed-waveguide grating.

***Response to Arguments***

4. Applicant's arguments filed 03/05/2004 have been fully considered but they are not persuasive.

The applicant's arguments claims 1-6 are not persuasive. The independent claim 1 is now amended to include the limitation of " **K group delay controllers comprising lattice-form optical circuits (K: natural number, K<N)**" and the applicant argues that Taga and Jinguji references fail to teach such limitation and applicant argues that the combination of Taga and Jinguji would provide a teaching of a K=N relationship, where the lattice-form variable group delay dispersion equalizer of Jinguji is incorportated into the dispersion slope equalizer of Taga. The examiner respectfully disagrees. Although Jinguji does not specifically teach K group delay controllers comprising lattice-form optical circuits connected to N waveguides (K: natural number, K<N). However, Jinguji clearly teaches a lattice-form variable group delay dispersion equalizer has two inputs (5,6) and two outputs (7,8)(as indicated in Fig. 3, column 3, lines 50-67 and col. 4, lines 1-14). Whether to use one input and one output of a lattice-form variable group delay dispersion equalizer connect to one waveguide (where K lattice-form variable group delay dispersion equalizers = N waveguides with K=N) or to use two inputs and two

outputs of a lattice-form variable group delay dispersion equalizer connect to two waveguides (where K lattice-form variable group delay dispersion equalizers = N/2 waveguides with K<N) would have been within the knowledge of a person having ordinary skill in the art and would have been an obvious engineering design choice. Therefore, it would have been obvious to obtain K group delay controllers comprising lattice-form optical circuits connected to N waveguides (K: natural number, K<N) in order to allow the amount of dispersion equalizers used can be cut down, reducing the size, weight and cost of the system.

Therefore, it is believed that the limitations of claims 1-6 are still met by the combination of Taga and Jinguji and the rejection is still maintained.

***Conclusion***

**5. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh Phan whose telephone number is (703)306-5840.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan, can be reached on (703)305-4729. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-4700.

Hanh Phan

05/11/2004